Speeding AM335x Programmable Realtime Unit (PRU) Application Development Through Improved Debug Tools

The hardware modules and descriptions referred to in this document are ***NOT SUPPORTED*** by Texas Instruments (www.ti.com / e2e.ti.com).

These materials are intended for do-it-yourself (DIY) users who want to use the PRU at their own risk without TI support. "Community" support is offered at BeagleBoard.org/discuss.





Agenda

- Introduction to the PRU Subsystem (PRU-ICSS on AM335x)
- Chip-level and Subsystem Level over of the PRU-ICSS
- PRU debug capabilities now included in CCS with details on how to use them
- PRU Resources





Introduction to the PRU SubSystem

- What is PRU SubSystem?
 - Programmable Real-time Unit SubSystem
 - Dual 32bit RISC processors
 - Local instruction and data RAM; access to SoC resources.
- What devices include PRU SubSystem?
 - Legacy PRUSS: OMAPL137/ AM17x, OMAPL138/ AM18x, C674x
 - PRU-ICSS* (PRUSSv2): AM335x
- Why PRU SubSystem?
 - Full programmability allows adding customer differentiation
 - Efficient in performing embedded tasks that require manipulation of packed memory mapped data structures
 - Efficient in handling of system events that have tight real-time constraints.

* PRU-ICSS = **P**rogrammable **R**eal-time **U**nit and **I**ndustrial **C**ommunication **S**ub**S**ystem.





PRU Subsystem Is / Is-Not

IS	IS-Not
Dual 32-bit RISC processor specifically designed for manipulation of packed memory mapped data structures and implementing system features that have tight real time constraints	In not a H/W accelerator to speed up algorithm computations .
IS Dual 32-bit RISC processor specifically designed for manipulation of packed memory mapped data structures and implementing system features that have tight real time constraints Simple RISC ISA - Approximately 40 instructions - Logical, arithmetic, and flow control ops all complete in a single cycle Could be used to enhance the existing peripheral feature set or implement new peripheral capability with software bit bang Includes example code to demonstrate various features. Examples can be used as building block	Is not a general purpose RISC processor - No multiply hardware/instructions - No cache
- Logical, arithmetic, and flow control ops all complete in a single cycle	 No pipeline No C programming
Could be used to enhance the existing peripheral feature set or implement new peripheral capability with software bit bang	Is not a stand alone configurable peripheral and will need some hardware assist for configurable peripheral implementation
Includes example code to demonstrate various features. Examples can be used as building blocks.	No Operating System or high level application software stack





PRU Value

- Extend connectivity and peripheral capability
 - Implement Industrial Communications protocols (like EtherCAT[®], PROFINET, EtherNet/IP[™], PROFIBUS, POWERLINK, SERCOS III)
 - Implement special peripherals and bus interfaces (like soft UARTs interfaces)
 - Digital IOs with latency in ns
 - Implement smart data movement schemes (especially useful for audio algorithms like reverb, room correction, etc.)
- Reduce system power consumption
 - Allows switching off both ARM and DSP clocks
 - Implement smart power controller by evaluating events before waking up DSP and/or ARM. Maximized power down time.
- Accelerate system performance
 - Full programmability allows custom interface implementation
 - Specialized custom data handling to offload CPU





Chip-level Integration of the PRU-ICSS (PRUSSv2)

- ARM has access to PRU-ICSS memory
- PRU-ICSS has access to its own local memories and other chip-level memory resources and peripherals







PRU-ICSS (PRUSSv2) Block Diagram



* On AM335x, only 15 General-Purpose Outputs and 16 General-Purpose Inputs are pinned out.





PRU Development Support Integrated in CCS

		CCS 5.x
pasm (PRU assembler)		No
AM335x PRU Debug Tools	Disassembly window	Yes
	Memory windows	Yes
	Register windows	Yes
	Execution controls	Yes
	Soft reset control	Yes
	Sleep control	Yes

Download the CCS 5.x here:

http://processors.wiki.ti.com/index.php/Download CCS





Summary of PRU Debug Capabilities

- <u>Disassembly window</u> to show PRU assembly code
- <u>Memory windows</u> to show PRU program and data memory contents
 - Ability to load/fill memory contents
 - Ability to save memory contents
 - Ability to load PRU code binaries
- <u>Register windows</u> to show PRU subsystem control, data and status registers
 - View and modify PRU subsystem registers
- Execution controls
 - Run/Halt
 - Single-stepping through assembly instructions
 - Breakpoint control
- PRU soft reset control





How to create a target configuration [1]

- You must choose the correct target configuration for CCS to include the PRU debug capabilities
- To create a new target configuration:
 - Open CCS
 - Click on Target > New Target Configuration...
 - CCS will open a New Target Configuration window, in this window:
 - Type the desired filename for the target configuration (like MyTargetConfig.ccxml)
 - If the storage location is correct, the click Finish.

😵 New Target Configuration 🛛 🔀
Target Configuration Create a new Target Configuration file.
File name: MyNewTargetConfigiccxml
Use shared location
Location: C:\Documents and Settings\a0321620\user\CCSTargetConFigurations Workspace
7 Finish Cancel





How to create a target configuration [2]

- In the main screen, CCS will open a "New Target Configuration" tab
 - In the Connection menu, choose the correct <u>emulator</u> you plan to use. The debug tools do not apply to the simulator.
 - In the Device box, choose AM335x from the options.
 - Click on the Save button under Save Configuration.

Basic	(1) Select the er	nulator
General Setup This section desc	rribes the general configuration about the target.	Advanced Setup
Connection	Blackhawk USB560-M Emulator	Target Configuration: lists the configuration options for the target.
Board or Device	AM33 🧟	Save Configuration
	(2) Select AM335x as the device	Test Connection To test a connection, all changes must have been saved, the configuration file contains no enors and the connection type supports this function. Test Connection (3) Save the configuration
	AM335×	





- Start a debug session:
 - Click on Target > Launch TI Debugger or click on the
 - CCS will connect to the target
- The Debug window will now show 4 disconnected targets:
 - The M3_wakeupSS_1 core
 - The CortexA8 core
 - The PRU0 core
 - The PRU1 core







- Select Disconnected Device on the CortexA8 and either:
 - Right-click and then select Connect Target, or
 - Use Target > Connect Target from the Menu on top
- CCS will connect to the CortexA8 and the Register, Disassembly and Memory windows will populate.

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Blackhawk USB560-M Emulator_0/M3_wakeupS5_1 (Disconnected : Unknown)	Name Value
■ 0x000233F8 (no symbols are defined for 0x000233F8)	Core Registers
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- Load AM335x CortexA8 and PRU gel files
 - Tools → GEL Files
 - Right click in GEL Files box and load AM335x_15x15_EVM.gel
 - Right click in GEL Files box and load AM335x_PRU_ICSS.gel

E Console E GEL Files 🔀					
 Console GEL Files X type filter text Memory Map GEL Files ARM Advanced Features Generic Debugger Options Cortex A8 Disassembly Style Options 	GEL Files (Cortex_A8) ⑦				
	Script	Status			
	AM335x_15x15_EVM.gel	Success			
	AM335x_PRU_ICSS.gel	Success			
Cortex A8 Disassembly Style Options					

Run the AM335x System Initialization script







Run the PRU_ICSS_Init script

beagleboard.org



- Select Disconnected Device on the PRU core and either:
 - Right-click and then select Connect Target, or
 - Use Target > Connect Target from the Menu on top
- CCS will connect to the PRU core and the Register, Disassembly and Memory windows will populate.





The Register Window

- When one of the connected PRUs is selected in the Debug Window, the Registers Window will show the Core Registers and Debug Registers for that PRU. You can expand and hide the Core and Debug registers in groups.
- You can modify values directly in the register window by double-clicking on the value and entering the new value.

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Name	Value								
 									
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The Register Window

- You can choose a register in the Register window and go to the memory address in the register:
 - Select the desired register
 - Right-click and select Open Memory View at Register Value
 - The Memory Window will go to the address specific in the selected register

The Register Window

- You can also choose a register to be a watch value in the Watch window:
 - Select the desired register
 - Right-click and select Create Watch Expression
 - The selected register is now a watch value in the Watch Window
 - You can put watch values from multiple CPUs in the same window, but CCS will only display the contents for the CPU selected in the debug window.

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The Memory Window

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Loading a PRU Binary (executable file)

- To load a PRU binary, it must be loaded through the Memory Window (unlike other CPUs in CCS).
 - Go to the Memory Window, pull down the menu for 🙍
 - Select Load, select the binary file you want to load, then click on Next
 - In the next window...
 - Enter the Start Address (usually 0x0)^[see note 1]
 - Choose Program Memory as the Memory Page
 - Choose 32-bits as the Type Size
 - Click Finish
- The binary is now loaded and if you go to the Disassembly window, you will see the code.

[Note 1] The PRU assembler always assembles code to start at program address 0x0. But you could do code overlays by modifying code to start at another address. In this case, you would use some address other than 0x0 for the binary being loaded.





The Disassembly Window

	Disa Instr	ssemblec uctions		Single-Step Controls
	📰 Disassembly 🗙	Memory (1)	0x0	✓ Q. (* 1. * 1. * 1. * 1. * 1. * 1. * 1. *
	♦ 0x00000000:	24000082	LDI R2.w0, #0	
	0x00000001: 0x00000002:	24000002 1E82FEFE	LDI R2.W2, #U SET R30, R30, R2.WO	
Address	0x00000 03:	0101C2C2	ADD R2.w2, R2.w2, #1	
	0x0 00004:	67FFC2FF	QBGT (0x3), R2.w2, #255	
\frown	0x00000005:	1082FEFE 01018282	LLR R30, R30, R2.w0 ADD R2.w0. R2.w0. #1	
Memory	0x00000007:	670882FB	QBGT (0x2), R2.w0, #8	
Contents	0x0000008:	2A000000	HALT	
(OPCODE)	0x00000009:	44444444 777777777	LBBU R31.63, R31, #255, 63 LBBO R31.63, R31, #255, 63	
	0x0000000B:	FFFFFFFF	LBBO R31.b3, R31, #255, b3	
	0x0000000C:	FFFFFFFF	LBBO R31.b3, R31, #255, b3	
	0x000000D:	FFFFFFFF	LBBO R31.b3, R31, #255, b3	
	0x0000000E:	FFFFFFFF	LBBO R31.b3, R31, #255, b3	
	0x0000000F:	FFFFFFFFF FFFFFFF	LBBU R31.b3, R31, #255, b3	
	0x00000011:	1111111 77777777	LBBO R31.D3, R31, #253, D3 LBBO R31 h3 R31 #255 h3	
	0x00000012:	FFFFFFFF	LBBO R31.b3, R31, #255, b3	
	0x00000013:	FFFFFFFF	LBBO R31.b3, R31, #255, b3	
	0+00000014		TEEN NOI NO NOI MOLE NO	

- Both single-step controls do the step through a single assembly instruction
- Not all of the controls in the disassembly window have a function on the PRU





Execution Control – Run, Halt, Single-Step

- To Run/Halt, with the PRU selected
 - Click the RUN button
 in the Debug window, or
 - Click Target > Run
- The PRU code will run until it is halted or executes a HALT instruction
- To single-step through code, use any of the single step controls.
 - Step-Into, Step-Over, Assembly Step-Into, Assembly Step-Over all have identical functions on the PRU





Execution Control – Breakpoint Control

- You can set/clear breakpoints by double-clicking in the bar to the left of the address in the disassembly window.
- You can also view/control PRU breakpoints by using View > Breakpoints





Execution Control Screenshot

beagleboard.org

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0×0000000	12 (no symbols are	e defined for 0x0	0000002)			888 R2	0x5BCBB777	Core Reg	ister: R2 Re	
🔤 📈 🖗 Blackhawk USB	560-M Emulator_0,	/PRU_1 (Disconn	ected : Unknow	n)		888 R3	0x697D84EA	Core Reg	ister: R3 Re	
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PRU-ICSS Documentation and Resources

- CCS External Download at http://processors.wiki.ti.com/index.php/Download_CCS
- AM335x PRU-ICSS Documentation is available in the AM335x PRU-ICSS package



